IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 16102US01

In the Application of:

Louis Jacobus Botha

U.S. Serial No.: 09/873,316

Filed: June 5, 2001

For: SYSTEM AND METHOD FOR DE-INTERLEAVING DATA IN A WIRELESS RECEIVER

Examiner: Chuong T. Ho

Group Art Unit: 2616

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/Michael T. Cruz/
Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal was *received* by the United States Patent and Trademark Office on January 30, 2007 for the above-identified patent application. A Petition for a Two-Month Extension is enclosed, thereby extending the deadline by which to file an Appeal Brief to May 30, 2007.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 5300 California Avenue, Irvine, California 92617, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals or interferences pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1, 3-6, 9, 11-15 and 17-23 are pending and are being prosecuted in the present application. Claims 2, 7, 8, 10 and 16 have been cancelled without prejudice. Claims 1, 3-6, 9, 11-15 and 17-23 stand rejected. The rejection of claims 1, 3-6, 9, 11-15 and 17-23 is being appealed.

STATUS OF AMENDMENTS

A Response After Office Action Made Final was filed November 14, 2006. No amendments to the application were made in the Response After Office Action Made Final. In response thereto, an Advisory Action was mailed on December 26, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Some embodiments according to some aspects of the present invention may provide, for example, system that de-interleaves data in a wireless receiver as set forth, for example, in claim 1. The system may include, for example, a memory buffer and unified means that perform a first and second de-interleaving of the data stored in the memory buffer. The memory buffer may be divided into logical partitions representing

radio frame blocks and physical channel blocks. Each radio frame block may store a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks. The single memory buffer may include, for example, a separate single-ported memory device for each radio frame block. The unified means may be coupled to the memory buffer and may include, for example, means for reading and writing the data to the memory buffer in connection with the first and second de-interleaving. The means may apply a first portion of a second de-interleaving pattern as data is written to the memory buffer and may apply a second portion of the second de-interleaving pattern as data is read from the memory buffer.

Some embodiments according to some aspects of the present invention may provide, for example, a receiver that receives data via a wireless link as set forth, for example, in claim 6. The receiver may include, for example, a decoding/demultiplexing unit. The decoding/demultiplexing unit may include, for example, a memory buffer and means for performing a first and second de-interleaving of the data. The memory buffer may store the data and may be divided logically into radio frame blocks and physical channel blocks. Each radio frame block may store a single radio frame of data. Each radio frame block may be divided into two or more of the physical channel blocks. The means for performing a first and second de-interleaving of the data may be coupled to the memory buffer and may include, for example, means for reading and writing the data to the memory buffer in connection with the first and second de-interleaving. The means may apply a first portion of a second de-interleaving pattern as the data is written into the memory buffer and may apply a second portion of the second de-interleaving pattern as the data is read from the memory buffer. The memory buffer may include, for example, a dual-ported memory device.

Some embodiments according to some aspects of the present invention may provide, for example, a system that de-interleaves data in a wireless receiver as set forth, for example, in claim 9. The system may include, for example, a memory buffer and a read/write unit. The memory buffer may be divided logically into radio frame blocks and physical channel blocks. Each radio frame block may store a single radio frame of data.

Each radio frame block may be divided into two or more of the physical channel blocks. The read/write unit may be coupled to the memory buffer and may be configured to perform a first and second de-interleaving of the data. The read/write unit may apply a first portion of a second de-interleaving pattern as the data is written to the memory buffer and may apply a second portion of the second de-interleaving pattern as the data is read from the memory buffer. The memory buffer may include, for example, multiple memory devices in which logical divisions do not correspond to physical divisions between the devices.

Some embodiments according to some aspects of the present invention may provide, for example, a method that de-interleaves data in a wireless receiver as set forth, for example, in claim 11. The method may include, for example, one or more of the following: logically divided a memory buffer into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks; applying a first portion of a second de-interleaving pattern as the data is written into the memory buffer, the data being written into a rectangular matrix; applying a second portion of the second de-interleaving pattern as the data is read from the memory buffer; and performing a first de-interleaving on the data.

Some embodiments according to some aspects of the present invention may provide, for example, a method as set forth, for example, in claim 13. The method may include, for example, one or more of the following: demodulating data received via a wireless link; storing the demodulated data in a memory buffer, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks; writing the data to the memory buffer to effectively perform a first portion of a second de-interleaving pattern; reading the data from the memory buffer to form an output data stream; and decoding the output data stream. The reading may effectively perform a second portion of a second de-interleaving pattern and a first de-interleaving pattern.

Some embodiments according to some aspects of the present invention may provide, for example, a system that de-interleaves data received at a wireless receiver as set forth, for example, in claim 15. The system may include, for example, a demodulator, a memory buffer and means for performing a first and second de-interleaving of the data stored in the memory buffer. The demodulator may be configured to demodulate the data. The memory buffer may be coupled to the demodulator and may store the data. The memory buffer may be divided logically into radio frame blocks and physical channel blocks. Each radio frame block may store a single radio frame of data. Each radio frame block may be divided into two or more of the physical channel blocks. The means for performing a first and second de-interleaving of the data stored in the memory buffer may be coupled to the memory buffer. The means may include, for example, means for reading and writing the data to the memory buffer in connection with the first and second de-interleaving and may perform a first portion of the second de-interleaving as the data is written into the memory buffer and may perform a second portion of the second de-interleaving and the first de-interleaving as the written data is read from the memory buffer.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 3-6, 9, 11-15 and 17-23 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,624,767 B1 to Da-Shan Shiu et al. ("Shiu") in view of United States Patent No. 6,971,057 B1 to Marc Delvaux et al. ("Delvaux").

ARGUMENT

I. CLAIMS 13 AND 14

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being obvious over Shiu in view of Delvaux. Appellant respectfully requests that the Board reverse the rejection.

Claim 13 recites "storing the demodulated data in a memory buffer, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each

radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks".

In the Office Action Made Final mailed September 14, 2006 ("Office Action Made Final"), the Examiner alleges that Shiu teaches these elements of claim 13 at col. 7, lines 1-5 and col. 15, lines 33-35. Office Action Made Final at page 18. Appellant respectfully disagrees.

It is apparent, especially in view of the citation to col. 15, lines 33-35 of Shiu that the Examiner is alleging that the "radio frame interval" in Shiu is the "radio frame block" as set forth in claim 13. Claim 13 recites "each radio frame block being divided into two or more of the physical channel blocks". Shiu at col. 15, lines 33-35 states "For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored".

It appears that the Examiner is equating "radio frame block" and "radio frame interval". FIG. 3 of Shiu illustrates radio frame intervals: n to n+1; n+1 to n+2; n+2 to n+3; etc. For example, in radio frame interval from n+2 to n+3, there are three physical channels PhCH#1, PhCH#2 and PhCH#3. Note that memory bank n+2 is associated with the radio time interval from n+2 to n+3. However, also note that memory bank n+2 stores all three radio frames 1A3, 2B2 and 3A1.

As set forth in claim 13, each radio frame block stores a single radio frame of data and is divided into two or more physical channel blocks. As alleged by the Examiner, radio frame 1A3 would have to be divided into two or more physical channel blocks. However, FIG. 3, claim 13 at col. 7, lines 1-5 and col. 15, lines 33-35 of Shiu teach each radio frame block storing a single radio frame of data and being divided into two or more physical channel blocks.

Delvaux does not make up for the teaching deficiencies of Shiu. Accordingly, the obviousness rejection based on Shiu in view of Delvaux cannot be maintained.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 13 and its rejected dependent claim (i.e., claim 14).

Claim 13 recites "writing said data to said memory buffer to effectively perform a first portion of a second de-interleaving pattern" and "wherein said reading effectively performs a second portion of a second de-interleaving pattern and a first de-interleaving pattern".

There is probably agreement that Shiu does not teach at least these elements as set forth in claim 13.

There is also probably agreement that Delvaux does not teach at least these elements as set forth in claim 13.

Instead, the Examiner is alleging that the modification of Shiu in view of Delvaux would have been obvious. Appellant strongly disagrees with such an allegation.

The Examiner pointed out, very early in the prosecution of the present application that Shiu describes that the second de-interleaving 252 is completely achieved by writing the symbols to buffer 512 in a permutated order that is complementary to that performed for the second interleaving 238. See, e.g., col. 13, lines 61-41 and FIG. 2B of Shiu.

The Examiner stated "A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be *efficiently achieved* by properly managing buffer 512. Specially, the second de-interleaving 252 can be *achieved* by writing the symbols to buffer 512 in a second permutated order that is complementary to that perform for the second interleaving 238". Office Action mailed March 25, 2004 at page 3 (italics added).

Thus, by the Examiner's own understanding of the teachings of Shiu, Shiu teaches that the second de-interleaving pattern is *completely* and *efficiently* achieved by writing to buffer 512.

Despite Shiu teaching *completely* achieving the second de-interleaving pattern in writing to buffer 512 (as previously alleged by the Examiner earlier in the prosecution of the present application) and despite the Examiner admitting that the second de-interleaving pattern is *efficiently* achieved by writing to buffer 512, the Examiner now states for the Board's review that it would have been obvious to break up the *completed*

second de-interleaving of Shiu and to break up the *efficient* second de-interleaving previously relied upon by the Examiner.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving (Examiner's characterization) of Shiu and add extra circuitry to the second de-interleaving 252 of Shiu.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving of Shiu (Examiner's characterization) and add extra steps to the second de-interleaving 252 of Shiu.

In short, even though Shiu teaches a second de-interleaving 252 that the Examiner previously considered *complete* and *efficient*, the Examiner's contention now is that one of ordinary skill in the art would add extra steps to an already completed second de-interleaving and that one of ordinary skill in the art would add extra circuitry to an already completed process to perform extraneous steps.

On its face, the Examiner's contention is to add extra steps to a single-step process in Shiu which the Examiner has already declared to be *efficient*. Adding extra and unneeded steps to a single-step process or adding extra steps after an already completed process would be *inefficient*.

It is respectfully submitted that one of ordinary skill in the art would not consider adding extra operations or steps or unnecessary circuitry to the *already completed* and *efficient* (Examiner's characterization) second de-interleaving 252 of Shiu.

In view of Shiu, one of ordinary skill in the art would have accomplished the second de-interleaving 252 by the single step of writing the symbols to buffer 512 in a permutated order.

It is respectfully submitted that one of ordinary skill in the art would not add extraneous or superfluous operations or unnecessary circuitry to the second de-interleaving 252 of Shiu since Shiu *already completely accomplishes* the second de-interleaving 252 in a single step of writing the symbols to buffer 512 in a permutated order. A single-step second de-interleaving 252 that the Examiner has previously characterized as *efficient*.

It is respectfully submitted that one of ordinary skill in the art would not have modified the *already completed* and *efficient* second de-interleaving 252 of Shiu with the alleged teachings of Delvaux.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 13 and its rejected dependent claim (i.e., claim 14).

II. CLAIM 6

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being obvious over Shiu in view of Delvaux. Appellant respectfully requests that the Board reverse the rejection.

Claim 6 recites "a memory buffer to store the data, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks".

In the Office Action Made Final, the Examiner alleges that Shiu teaches these elements of claim 6 at col. 7, lines 1-5 and col. 15, lines 33-35. Office Action Made Final at page 4. Appellant respectfully disagrees.

It is apparent, especially in view of the citation to col. 15, lines 33-35 of Shiu that the Examiner is alleging that the "radio frame interval" in Shiu is the "radio frame block" as set forth in claim 6. Claim 6 recites "each radio frame block being divided into two or more of the physical channel blocks". Shiu at col. 15, lines 33-35 states "For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored".

It appears that the Examiner is equating "radio frame block" and "radio frame interval". FIG. 3 of Shiu illustrates radio frame intervals: n to n+1; n+1 to n+2; n+2 to n+3; etc. For example, in radio frame interval from n+2 to n+3, there are three physical channels PhCH#1, PhCH#2 and PhCH#3. Note that memory bank n+2 is associated with the radio time interval from n+2 to n+3. However, also note that memory bank n+2 stores all three radio frames 1A3, 2B2 and 3A1.

As set forth in claim 6, each radio frame block stores a single radio frame of data and is divided into two or more physical channel blocks. As alleged by the Examiner, radio frame 1A3 would have to be divided into two or more physical channel blocks. However, FIG. 3, claim 13 at col. 7, lines 1-5 and col. 15, lines 33-35 of Shiu teach each radio frame block storing a single radio frame of data and being divided into two or more physical channel blocks.

Delvaux does not make up for the teaching deficiencies of Shiu. Accordingly, the obviousness rejection based on Shiu in view of Delvaux cannot be maintained.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 6.

Claim 6 recites "wherein said means applies a first portion of a second de-interleaving pattern as the data is written into the memory buffer" and "wherein said means applies a second portion of said second de-interleaving pattern as the data is read from the memory buffer".

There is probably agreement that Shiu does not teach at least these elements as set forth in claim 6.

There is also probably agreement that Delvaux does not teach at least these elements as set forth in claim 6.

Instead, the Examiner is alleging that the modification of Shiu in view of Delvaux would have been obvious. Appellant strongly disagrees with such an allegation.

The Examiner pointed out, very early in the prosecution of the present application that Shiu describes that the second de-interleaving 252 is completely achieved by writing the symbols to buffer 512 in a permutated order that is complementary to that performed for the second interleaving 238. See, e.g., col. 13, lines 61-41 and FIG. 2B of Shiu.

The Examiner stated "A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be *efficiently achieved* by properly managing buffer 512. Specially, the second de-interleaving 252 can be *achieved* by writing the symbols to

buffer 512 in a second permutated order that is complementary to that perform for the second interleaving 238". Office Action mailed March 25, 2004 at page 3 (italics added).

Thus, by the Examiner's own understanding of the teachings of Shiu, Shiu teaches that the second de-interleaving pattern is *completely* and *efficiently* achieved by writing to buffer 512.

Despite Shiu teaching *completely* achieving the second de-interleaving pattern in writing to buffer 512 (as previously alleged by the Examiner earlier in the prosecution of the present application) and despite the Examiner admitting that the second de-interleaving pattern is *efficiently* achieved by writing to buffer 512, the Examiner now states for the Board's review that it would have been obvious to break up the *completed* second de-interleaving of Shiu and to break up the *efficient* second de-interleaving previously relied upon by the Examiner.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving (Examiner's characterization) of Shiu and add extra circuitry to the second de-interleaving 252 of Shiu.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving of Shiu (Examiner's characterization) and add extra steps to the second de-interleaving 252 of Shiu.

In short, even though Shiu teaches a second de-interleaving 252 that the Examiner previously considered *complete* and *efficient*, the Examiner's contention now is that one of ordinary skill in the art would add extra steps to an already completed second de-interleaving and that one of ordinary skill in the art would add extra circuitry to an already completed process to perform extraneous steps.

On its face, the Examiner's contention is to add extra steps to a single-step process in Shiu which the Examiner has already declared to be *efficient*. Adding extra and unneeded steps to a single-step process or adding extra steps after an already completed process would be *inefficient*.

It is respectfully submitted that one of ordinary skill in the art would not consider adding extra operations or steps or unnecessary circuitry to the *already completed* and *efficient* (Examiner's characterization) second de-interleaving 252 of Shiu.

In view of Shiu, one of ordinary skill in the art would have accomplished the second de-interleaving 252 by the single step of writing the symbols to buffer 512 in a permutated order.

It is respectfully submitted that one of ordinary skill in the art would not add extraneous or superfluous operations or unnecessary circuitry to the second de-interleaving 252 of Shiu since Shiu *already completely accomplishes* the second de-interleaving 252 in a single step of writing the symbols to buffer 512 in a permutated order. A single-step second de-interleaving 252 that the Examiner has previously characterized as *efficient.*

It is respectfully submitted that one of ordinary skill in the art would not have modified the *already completed* and *efficient* second de-interleaving 252 of Shiu with the alleged teachings of Delvaux.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 6.

III. CLAIM 9

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being obvious over Shiu in view of Delvaux. Appellant respectfully requests that the Board reverse the rejection.

Claim 9 recites "memory buffer divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks".

In the Office Action Made Final, the Examiner alleges that Shiu teaches these elements of claim 6 at col. 7, lines 1-5 and col. 15, lines 33-35. Office Action Made Final at page 11. Appellant respectfully disagrees.

It is apparent, especially in view of the citation to col. 15, lines 33-35 of Shiu that the Examiner is alleging that the "radio frame interval" in Shiu is the "radio frame block"

as set forth in claim 9. Claim 9 recites "each radio frame block being divided into two or more of the physical channel blocks". Shiu at col. 15, lines 33-35 states "For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored".

It appears that the Examiner is equating "radio frame block" and "radio frame interval". FIG. 3 of Shiu illustrates radio frame intervals: n to n+1; n+1 to n+2; n+2 to n+3; etc. For example, in radio frame interval from n+2 to n+3, there are three physical channels PhCH#1, PhCH#2 and PhCH#3. Note that memory bank n+2 is associated with the radio time interval from n+2 to n+3. However, also note that memory bank n+2 stores all three radio frames 1A3, 2B2 and 3A1.

As set forth in claim 9, each radio frame block stores a single radio frame of data and is divided into two or more physical channel blocks. As alleged by the Examiner, radio frame 1A3 would have to be divided into two or more physical channel blocks. However, FIG. 3, claim 13 at col. 7, lines 1-5 and col. 15, lines 33-35 of Shiu teach each radio frame block storing a single radio frame of data and being divided into two or more physical channel blocks.

Delvaux does not make up for the teaching deficiencies of Shiu. Accordingly, the obviousness rejection based on Shiu in view of Delvaux cannot be maintained.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 9.

Claim 9 recites "wherein the read/write unit applies a first portion of a second de-interleaving pattern as the data is written to the memory buffer" and "wherein the read/write unit applies a second portion of said second de-interleaving pattern as the data is read from the memory buffer".

There is probably agreement that Shiu does not teach at least these elements as set forth in claim 9.

There is also probably agreement that Delvaux does not teach at least these elements as set forth in claim 9.

Instead, the Examiner is alleging that the modification of Shiu in view of Delvaux would have been obvious. Appellant strongly disagrees with such an allegation.

The Examiner pointed out, very early in the prosecution of the present application that Shiu describes that the second de-interleaving 252 is completely achieved by writing the symbols to buffer 512 in a permutated order that is complementary to that performed for the second interleaving 238. See, e.g., col. 13, lines 61-41 and FIG. 2B of Shiu.

The Examiner stated "A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be *efficiently achieved* by properly managing buffer 512. Specially, the second de-interleaving 252 can be *achieved* by writing the symbols to buffer 512 in a second permutated order that is complementary to that perform for the second interleaving 238". Office Action mailed March 25, 2004 at page 3 (italics added).

Thus, by the Examiner's own understanding of the teachings of Shiu, Shiu teaches that the second de-interleaving pattern is *completely* and *efficiently* achieved by writing to buffer 512.

Despite Shiu teaching *completely* achieving the second de-interleaving pattern in writing to buffer 512 (as previously alleged by the Examiner earlier in the prosecution of the present application) and despite the Examiner admitting that the second de-interleaving pattern is *efficiently* achieved by writing to buffer 512, the Examiner now states for the Board's review that it would have been obvious to break up the *completed* second de-interleaving of Shiu and to break up the *efficient* second de-interleaving previously relied upon by the Examiner.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving (Examiner's characterization) of Shiu and add extra circuitry to the second de-interleaving 252 of Shiu.

It is now the Examiner's contention that one of ordinary skill in the art would break up the complete and efficient second de-interleaving of Shiu (Examiner's characterization) and add extra steps to the second de-interleaving 252 of Shiu.

In short, even though Shiu teaches a second de-interleaving 252 that the Examiner previously considered *complete* and *efficient*, the Examiner's contention now is that one of ordinary skill in the art would add extra steps to an already completed second de-interleaving and that one of ordinary skill in the art would add extra circuitry to an already completed process to perform extraneous steps.

On its face, the Examiner's contention is to add extra steps to a single-step process in Shiu which the Examiner has already declared to be *efficient*. Adding extra and unneeded steps to a single-step process or adding extra steps after an already completed process would be *inefficient*.

It is respectfully submitted that one of ordinary skill in the art would not consider adding extra operations or steps or unnecessary circuitry to the *already completed* and *efficient* (Examiner's characterization) second de-interleaving 252 of Shiu.

In view of Shiu, one of ordinary skill in the art would have accomplished the second de-interleaving 252 by the single step of writing the symbols to buffer 512 in a permutated order.

It is respectfully submitted that one of ordinary skill in the art would not add extraneous or superfluous operations or unnecessary circuitry to the second de-interleaving 252 of Shiu since Shiu *already completely accomplishes* the second de-interleaving 252 in a single step of writing the symbols to buffer 512 in a permutated order. A single-step second de-interleaving 252 that the Examiner has previously characterized as *efficient*.

It is respectfully submitted that one of ordinary skill in the art would not have modified the *already completed* and *efficient* second de-interleaving 252 of Shiu with the alleged teachings of Delvaux.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claim 9.

IV. CLAIMS 1, 3-5, 11, 12, 15 AND 17-23

Claims 1, 3-5, 11, 12, 15 and 17-23 stand rejected under 35 U.S.C. § 103(a) as being obvious over Shiu in view of Delvaux. Appellant respectfully requests that the Board reverse the rejection.

Independent claims 1, 11 and 15 recite at least some language that is the same or similar to language recited in claims 6 or 9. Accordingly, Appellant respectfully makes the same or similar arguments, if appropriate, with respect to claims 11, 11 and 15 that were made with respect to claims 6 or 9.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection with respect to claims 1, 3-5, 11, 12, 15 and 17-23

V. CONCLUSION

For the foregoing reasons, it is believed that claims 1, 3-6, 9, 11-15 and 17-23 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection of claims 1, 3-6, 9, 11-15 and 17-23 is therefore respectfully requested, thereby placing claims 1, 3-6, 9, 11-15 and 17-23 in condition for allowance. Accordingly, issuance of a patent on the application is therefore respectfully requested.

The Commissioner is hereby authorized to charge any additional fees, to charge any fee deficiencies or to credit any overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: May 30, 2007

Respectfully submitted,

/Michael T. Cruz/
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CLAIMS APPENDIX

The following claims are involved in this appeal:

1. A system for de-interleaving data in a wireless receiver comprising:

a memory buffer divided into logical partitions representing radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks, the single memory buffer comprising a separate single-ported memory device for each radio frame block; and

unified means, coupled to said memory buffer, for performing a first and second de-interleaving of the data stored in said memory buffer, wherein said means includes means for reading and writing the data to the memory buffer in connection with said first and second de-interleaving,

wherein said means applies a first portion of a second de-interleaving pattern as data is written to the memory buffer, and

wherein said means applies a second portion of said second de-interleaving pattern as data is read from the memory buffer.

3. The system of claim 1, wherein said means performs said first de-interleaving as the stored data is read from said memory buffer.

4. The system of claim 1, wherein the data comprises radio frames and said means causes said radio frames to be stored in said radio frame blocks.

5. The system of claim 4, wherein the data is transmitted over one or more physical channels, wherein each of said radio frames comprises a physical channel frame associated with each physical channel, each of said radio frame blocks comprises a physical channel block associated with each physical channel, and said means causes said physical channel frames to be stored in said physical channel blocks.

6. A receiver that receives data via a wireless link, said receiver comprising:

a decoding/demultiplexing unit comprising:

a memory buffer to store the data, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks, and

means, coupled to said memory buffer, for performing a first and second de-interleaving of the data, wherein said means includes means for reading and writing the data to the memory buffer in connection with said first and second de-interleaving,

wherein said means applies a first portion of a second de-interleaving pattern as the data is written into the memory buffer,

wherein said means applies a second portion of said second de-interleaving pattern as the data is read from the memory buffer, and

wherein said memory buffer comprises a dual-ported memory device.

9. A system for de-interleaving data in a wireless receiver comprising:

a memory buffer divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks; and

a read/write unit, coupled to said memory buffer, wherein said read/write unit is configured to perform a first and second de-interleaving of the data,

wherein the read/write unit applies a first portion of a second de-interleaving pattern as the data is written to the memory buffer,

wherein the read/write unit applies a second portion of said second de-interleaving pattern as the data is read from the memory buffer, and

wherein the memory buffer comprises multiple memory devices in which logical divisions do not correspond to physical divisions between the devices.

11. A method for de-interleaving data in a wireless receiver comprising:

logically divided a memory buffer into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks;

applying a first portion of a second de-interleaving pattern as the data is written into the memory buffer, the data being written into a rectangular matrix;

applying a second portion of said second de-interleaving pattern as the data is read from the memory buffer; and

performing a first de-interleaving on the data.

12. The method of claim 11 further comprising:

reassembling one or more physical channels from the data stored in said memory buffer;

performing a second removal of discontinuous transmission indication bits from the data stored in said memory buffer;

demultiplexing the data stored in said memory buffer into a plurality of transport channels; and

reassembling transport blocks from the data stored in said memory buffer, wherein the data comprises radio frames.

13. A method comprising:

demodulating data received via a wireless link;

storing the demodulated data in a memory buffer, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks;

writing said data to said memory buffer to effectively perform a first portion of a second de-interleaving pattern;

reading said data from said memory buffer to form an output data stream; and

decoding said output data stream,

wherein said reading effectively performs a second portion of a second de-interleaving pattern and a first de-interleaving pattern.

14. The method of claim 13 further comprising:

reassembling one or more physical channels from the data stored in said memory buffer;

performing a second removal of discontinuous transmission indication bits from the data stored in said memory buffer;

demultiplexing the data stored in said memory buffer into a plurality of transport channels; and

reassembling transport blocks from the data stored in said memory buffer, wherein the data comprises radio frames.

15. A system for de-interleaving data received at a wireless receiver comprising:

a demodulator configured to demodulate the data;

a memory buffer, coupled to said demodulator, to store said data, the memory buffer being divided logically into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks; and

means, coupled to said memory buffer, for performing a first and second de-interleaving of the data stored in said memory buffer, wherein said means includes means for reading and writing the data to the memory buffer in connection with said first and second de-interleaving,

wherein said means performs a first portion of said second de-interleaving as the data is written into the memory buffer and said means performs a second portion of said second de-interleaving and said first de-interleaving as the written data is read from said memory buffer.

17. The system of claim 15, wherein said means performs said first de-interleaving as the written data is read from said memory buffer.

18. The system of claim 1, wherein the memory buffer is divided into at least nine logical partitions represents at least nine radio frame blocks.

19. The system according to claim 18, wherein said means can de-interleave data from eight radio frames while a ninth radio frame is being received.

20. The system according to claim 1, wherein the physical channel blocks are sized to accommodate a maximum physical channel frame size allowed by the system.

21. The system according to claim 1, wherein the physical channel blocks are each sized to accommodate 19,200 bits per physical channel.

22. The system according to claim 1, wherein the radio frame blocks are sized to handle a maximum frame size allowed by the system.

23. The system according to claim 13, wherein said reading further effectively performs reassembling physical channels and reassembling radio frames.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.